EE5219: Design and Application of Phase-Locked Loop

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Course Description:
This course introduces the design and analysis of the phase-locked loop (PLL). It covers the phase domain analysis and modeling of the loop, building blocks, phase noise evaluation of the PLL. It also includes the applications of the PLL, especially the clock and data recovery (CDR) design for the wireline receiver.

Prerequisites: Microelectronics

Textbook: Class Notes and Technical Papers

Teaching Method:
Lecture: 3 hours
Outside Study: 3 hours

References:
1. Design of Integrated Circuits for Optical Communications, B. Razavi, McGraw-Hill, 2003.
2. RF Microelectronics, B. Razavi, Prentice Hall, 1998.

Grading:
1. Homework: 40%
2. Final Exam: 30%
3. Final Project: 30%

Outline:
1. Phase Domain Analysis
2. Phase/Frequency Detector
3. Voltage-Controlled Oscillator
4. Frequency Divider
5. PLL Architecture
6. Clock and Data Recovery

*AI is not applicable in this course.