課綱上傳資料 (Syllabus Information for School System)

授課教師：張守仁教授
課程: 製程整合 (Process Integration)

1. **課程簡述 Brief Course Description**
   This course provides the basic introduction of process integration in semiconductor IC manufacturing, and the topics include Logic technology scaling, enablement of new technology nodes, process variation and design co-optimization, process flow in FEOL, MEoL, BEoL, and 3D package, and yield/reliability. Might cover the DRAM and emerging technologies.

2. **此科目對應之系所課程規畫所欲培養之核心能力**(Core capability to be cultivated by this course)：
   Build up the knowledge in the Logic and chiplet technology development from integration point of view.

3. **課程內容關鍵字(Key Words)**：
   Process integration, Logic Technology, CMOS, Process Flow, System Integration and 3D stacking.

4. **課程大綱 Detailed Course Syllabus**
   - 課程說明(Course Description):
     See Syllabus
   - 指定用書(Text Books):
     NA
   - 參考書籍(References):
     i. "Semiconductor physics and devices basic principles", Donald A. Neamen (ISBN-10 0073529583)
     ii. "Modern Semiconductor Devices for Integrated Circuits", Chenming Calvin Hu (ISBN-13 978-0137006687)
     iii. "Semiconductor Integrated Circuit Processing Technology", Revised version, by W. R. Runyan and K. E. Bean (ISBN-10 0201108313)
     iv. "Microchip Fabrication: A Practical Guide to Semiconductor Processing", Sixth Edition, by Van Zant, Peter (ISBN 10: 0071821015)
     v. "Semiconductor Microchips and Fabrication : A Practical Guide to Theory and Manufacturing", by Lian, Yaguang (ISBN 10: 1119867789)
     vi. "Solid State Electronic Device", seventh edition (ISBN-13: 9781292060552)

- 教學方式(Teaching Method):
  Lecture

- 教學進度(Syllabus):(Might be adjusted)

週次	授課內容
1	Semiconductor Material & Device Overview (I)
2	Semiconductor Material & Device Overview (I)
3	Platform Enablement – from design rules to product chips
4	Logic Technology Scaling and Roadmap
5	MOSFET and scaling
6	Process variability and Design-Technology Co-Optimization
7	FEoL and MEoL Integration (I)
8	FEoL and MEoL Integration (II)
Mid-term Exam and Homework Delivery	
9	BEoL Integration (Power Rail & TSV) (I)
10	BEoL Integration (Power Rail & TSV) (II)
11	Yield and Reliability
12	Stacking and Monolithic Technology (I)
13	Stacking and Monolithic Technology (II)
14	FinFET Technology brief introduction (I)
15	FinFET Technology brief introduction (II)
16	Architecture and Process for AI applications
17	*Final Report (Oral) I*
18	*Final Report (Oral) II*

- 成績考核(Evaluation):
  Mid-term Exam 20%
  Mid-term Homework 30%
  Final Report (Oral Presentation) 30%
  Final Exam 20%